

Investigation, Evaluation, and Optimization of Stray Inductance in Laminated Busbar

Cai Chen, Xuejun Pei, *Member, IEEE*, Yu Chen, *Member, IEEE*, and Yong Kang

Abstract—Wiring inductance has a critical effect on electrical, thermal, and electromagnetic compatibility (EMC) performances in inverters. Therefore, the low stray inductance laminated busbar, as a state-of-the-art pathway interface, is widely used in high-power inverters. However, the asymmetrical stray inductances of the laminated busbar may cause different voltage and thermal stresses for semiconductor devices of the same power stage. In order to achieve low and symmetrical stray inductances in the laminated busbar, this paper presents the investigation, evaluation, and optimization of the stray inductances of the laminated busbar. Based on the current commutation loop (CCL) analysis, the investigation of two-layer, three-layer, and multilayer laminated busbars is proposed through three-dimensional (3-D) finite element analysis (FEA) simulations. It can be found that the skin effect, mutual effect, CCL length, CCL separation distance, and split plate significantly influence the stray inductance of laminated busbars. Furthermore, the multilayer laminated busbar structure for multilevel neutral point clamped (NPC) inverter is derived. On the basis of the theoretical analysis, CCL stray inductances of a three-layer laminated busbar are extracted by means of FEA simulation and an improved impedance resonant measurement in a single-phase H-bridge high-power inverter. Insulated gate bipolar transistor (IGBT) voltage overshoot waveforms further validate the stray inductance asymmetry of the laminated busbar. A compromise between the stray inductance and symmetry is proposed in the three-layer laminated busbar. Finally, several feasible guidelines for the optimization of the laminated busbar design are introduced.

Index Terms—Current commutation loop (CCL), finite element analysis (FEA), impedance resonant, laminated busbar.

I. INTRODUCTION

DUE to the short turn-off time of insulated gate bipolar transistor (IGBT), the large voltage overshoot occurs across IGBT in high-power inverters. As a result, the high voltage stress may exceed the safe operating area (SOA) of semiconductor devices, ultimately causing the destruction of semiconductor devices. Consequently, the low stray inductance laminated busbar, a type of state-of-the-art pathway interface, is widely applied to

connect dc-link capacitors and semiconductor devices. The current commutation loop (CCL) stray inductance is related to dc-link capacitors, semiconductor devices, connection screws, and laminated busbar. In terms of the stray inductances associated with three former components, the value of stray inductances are intrinsic that cannot be easily reduced. Therefore, this paper mainly focuses on the reduction of the stray inductances of the CCL.

The low stray inductance laminated busbar can effectively restrain the voltage overshoot, electromagnetic interference (EMI), system resonance problems, and switching losses for high-power converters [1]–[8]. Several planar laminated busbar designs have been presented in different applications. For example, the laminated busbar for single-phase/ three-phase voltage source inverter, three-phase three-level neutral point clamped (NPC) inverter, and MVA-level H-bridge cascade multilevel inverter have been studied in [8]–[16].

The laminated busbar has been modeled by numerical analytical simulation tools, such as finite element analysis (FEA) [7], [8], [15], partial element equivalent circuit (PEEC) [12]–[14], [16], and measurement-based methods like time-domain reflectometry (TDR) [17]. The FEA method solves the Maxwell's differential field equations to obtain the stray parameters. The PEEC method divides the large size conductor into an appropriate number, resulting in fast simulation efficiency and less computer memory configurations. The TDR method requires the special hardware (TDR/sampling head) and software, in which the complicated experimental measurements are desired. Therefore, the FEA and PEEC methods are commonly used in the laminated busbar modeling.

Due to the high resolution requirements of measuring equipment, the direct measurement of stray inductance always exists unpredictable errors. In order to verify the modeling accuracy, some indirect measurement methods were used. A method based on the switch voltage overshoot ΔV and di/dt was presented, but this calculated result was the stray inductance of the whole circuit CCL [3], [15]. Another method is proposed to utilize the resonant capacitor to calculate the stray inductance [1], [8], [13]. However, due to the induced stray inductances (equivalent series inductance (ESL) of resonant capacitor, the stray inductances of connected copper strips and wires, etc.) were not considered, such kind of method results in more than 12% errors. This paper will introduce an improved step-by-step impedance resonant method, which can effectively weaken the influence of induced stray inductances.

Due to different converter topologies and power-levels, the mechanical layout structures of the laminated busbar are of great difference. To get the optimal design result, the laminated

Manuscript received July 12, 2013; revised September 9, 2013; accepted September 10, 2013. Date of current version February 18, 2014. This work was supported in part by the Delta Power Electronics Science and Education Development Plan (DREK2013001) and in part by the Fundamental Research Funds for the Central Universities of China (2012QN195). Recommended for publication by Associate Editor A. M. Trzynadlowski.

The authors are with the State Key Laboratory of Advanced Electromagnetic Engineering and Technology, Huazhong University of Science and Technology, Wuhan 430074, China (e-mail: hust.chencai@gmail.com; ppei215@mail.hust.edu.cn; ayu03@163.com; ykang@mail.hust.edu.cn).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TPEL.2013.2282621

busbar and converter topologies, should be fully considered. Unlike only one CCL existing in the buck converter [1], [3], there are more than one CCLs in the single-phase, three-phase, and multilevel inverters. Because of the asymmetry in spatial arrangements, components layouts, and laminated busbar structures, CCLs with asymmetrical stray inductances easily occur in the laminated busbar. As a result, additional snubber circuit and heat-sink are required to restrain the dissymmetrical voltage and thermal stresses. Hence, the stray inductance symmetry of CCLs deserves special considerations.

Several laminated busbars were designed and used in high power applications. In [3], [6], and [7], one CCL was discussed without the stray inductance symmetry consideration for a single-phase inverter. Reference [14] proposed a four-layer laminated busbar with multiple CCLs in a three-phase NPC three-level inverter. For design, the laminated busbar obviously has asymmetrical CCL stray inductances 78 and 208 nH, respectively. In [12] and [15], the asymmetry of CCL stray inductances also existed in NPC three-level inverters. The asymmetrical stray inductances of CCLs lead unequal voltage spikes to semiconductor devices. In order to obtain symmetrical CCL stray inductances, [18] and [19] used holes and apertures to equalize the stray inductances of CCLs. Unfortunately, this method increased stray inductances both of two CCLs. In [8], a tradeoff optimum three-layer laminated busbar was proposed by modifying the busbar structure, which achieved two symmetrical stray inductances of CCLs.

In this paper, the investigation, evaluation, and optimization of laminated busbar CCL stray inductance are presented. In Section II, asymmetrical CCLs are analyzed in a single-phase H-bridge inverter. Then, considering the skin effect, mutual effect, CCL length, CCL separation distance, and split plate, the investigation of two-layer, three-layer, and multilayer laminated busbars are introduced in Section III. In Section IV, the stray inductances of a three-layer laminated busbar are extracted by means of FEA simulation and an improved step-by-step impedance resonant measurement method in a single-phase H-bridge high-power inverter. Then, IGBT voltage overshoot measurements further verified the CCL stray inductances asymmetrical. Moreover, a compromised laminated busbar design scheme between the stray inductance and symmetry is proposed in the three-layer laminated busbar in Section V. Finally, a summary is given in Section VI.

II. STRAY INDUCTANCES OF CCLs IN CIRCUIT

Fig. 1 describes turn-off transients of four IGBTs in a typical single-phase H-bridge inverter. Taking T_1 turn-off process as an example, the load current I_L commutates from T_1 to T_2 free-wheeling diode (FWD) after receiving the gate turn-off signal. The turn-off process of T_1 can be simply divided into three stages as depicted in Fig. 1(a)–(c), and the relevant waveforms are sketched in Fig. 1(d). The operation processes are briefly discussed in the following.

Stage 1 [see Fig. 1(a)]: At t_0 , T_1 receives the turn-off signal. After a short turn-off delay time, the voltage v_{T1} rises, and the

current i_{T1} remains equal to the load current I_L during this stage.

Stage 2 [see Fig. 1(b)]: Once voltage v_{T1} reaches the dc supply voltage V_{dc} , i_{T1} decreases and i_{T2} rises at the same rate of di_{T1}/dt . Meanwhile, a voltage overshoot V_{p1} occurs across T_1 due to the circuit stray inductance, and the voltage overshoot V_{p1} is given as

$$V_{p1} = V_{dc} + l_1 \frac{di_{T1}}{dt} \quad (1)$$

where l_1 is the stray inductance of CCL1. In addition, the CCL consists of dc-link capacitors, T_1 , the FWD of T_2 , and laminated busbar, as depicted in CCL1 in Fig. 1(b). The stray inductance l_1 of CCL1 is composed by

$$l_1 = l_s + l_{busbar1} \quad (2)$$

where l_s is the sum of dc-link capacitor ESL, two IGBT stray inductances, and connecting screw stray inductances; $l_{busbar1}$ is the stray inductance of the laminated busbar. $l_{busbar1}$ can be divided into two parts l_{AB1} and l_{BC1} in Fig. 1(b), which are concerned with the laminated busbar structure and components layout.

Stage 3 [see Fig. 1(c)]: After t_2 , i_{T1} decreases to zero, and v_{T1} keeps at V_{dc} . In this stage, because of the stray inductance l_1 , the voltage oscillation often occurs, leading to the increase of the voltage stress and losses [2].

Similarly, turn-off processes of T_2 are described in Fig. 1(e)–(h). The CCL composed of dc-link capacitors, laminated busbar, T_2 , and T_1 FWD is also obtained in Fig. 1(f). The same voltage overshoot and the stray inductance can be expressed as (1) and (2), respectively.

However, turn-off processes of T_3 and T_4 shown in Fig. 1(i)–(p) are different from T_1 and T_2 for the different CCL2, as depicted in red color. This CCL has a different stray inductance l_2 for the dissimilar laminated busbar stray inductance $l_{busbar2}$, leading to the overshoot voltage as

$$V_{p2} = V_{dc} + l_2 \frac{di_{T3}}{dt} \quad (3)$$

where l_2 is the stray inductance of CCL2, as shown in Fig. 1(j) and (n). Also, the stray inductance l_2 of CCL2 can be given as

$$l_2 = l_s + l_{busbar2} \quad (4)$$

where $l_{busbar2}$ is the sum of l_{AB2} and l_{AD2} .

From (2) and (4), two CCL total stray inductances of dc-link capacitors, semiconductor devices, and connection screws have the same amount l_s . Therefore, the asymmetry of two CCL stray inductances is mainly caused by different CCL stray inductances $l_{busbar1}$ and $l_{busbar2}$ of the laminated busbar.

III. INVESTIGATION OF LAMINATED BUSBARS

Due to different inverter topologies, laminated busbars are designed into different layers. These CCLs with different laminated busbar layers are investigated in this section.

On the basis of the physical structure layout, the laminated busbar model is built in the FEA software Ansoft Maxwell 2-D/3-D [20]. The principle of this tool is based on Maxwell's

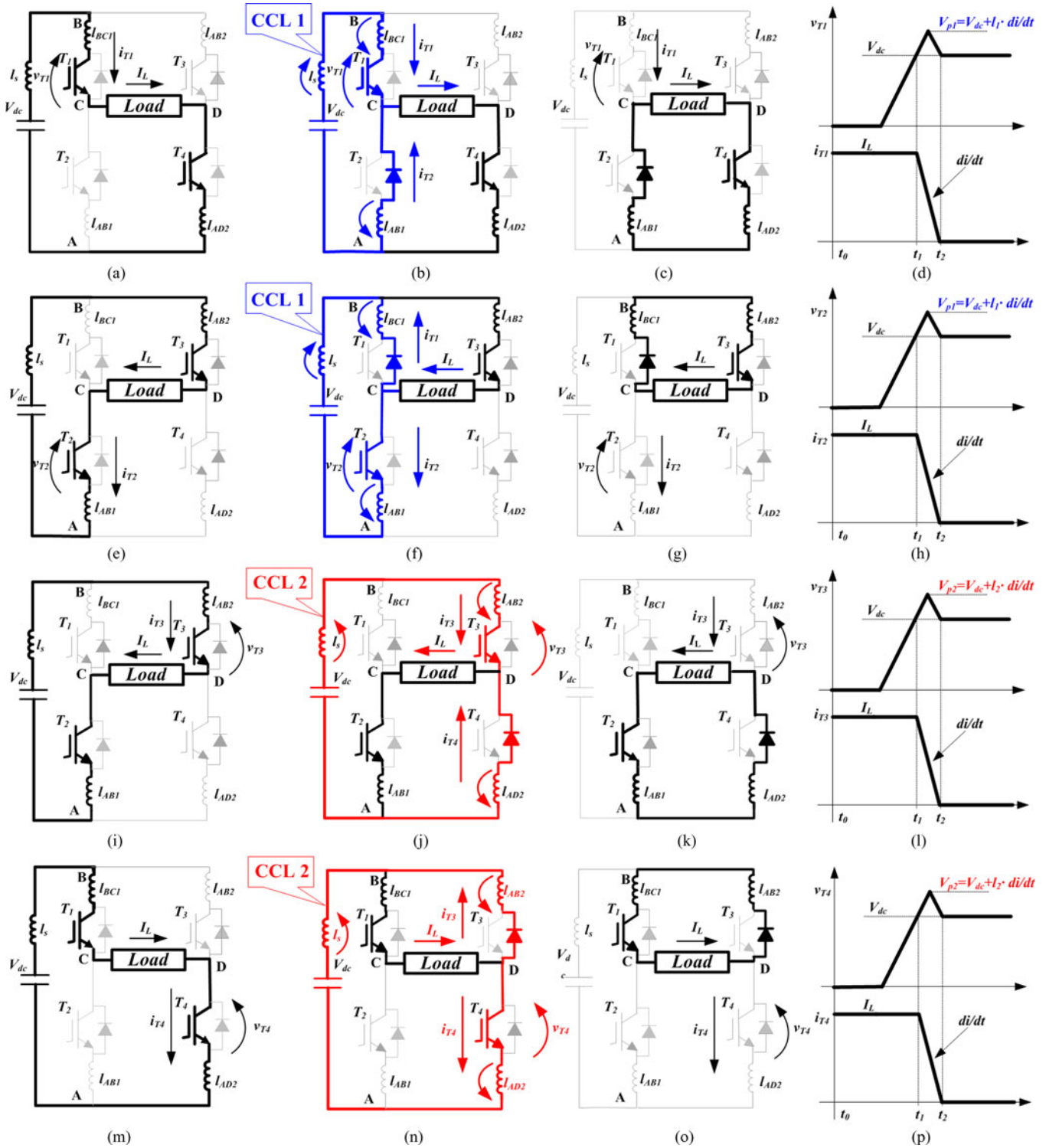


Fig. 1. Two CCLs of the single-phase H-bridge inverter during four IGBT turn-off transients.

differential field equations, thus it can accurately calculate stray parameters for complex laminated busbar structures [21].

A. Two-Layer Laminated Busbar

A two-layer laminated busbar with the CCL (the dotted line) is shown in Fig. 2. The model consists of two copper planar busbars

and an air-insulating layer, and laminated busbar dimensions are $a = 400$ mm, $b = 400$ mm, $T = 2$ mm. Under the certain busbar dimensions, only the length and insulation thickness of CCL significantly affect the loop stray inductance. The CCL length along y -direction is s and the CCL insulation thickness along z -direction is d . The stray inductance of CCL in terms of s and d can be obtained by varying these two parameters

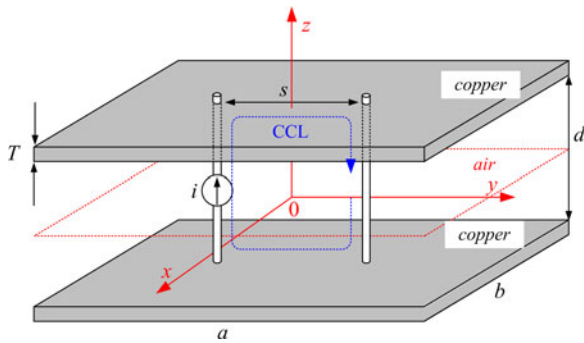


Fig. 2. Two-layer laminated busbar.

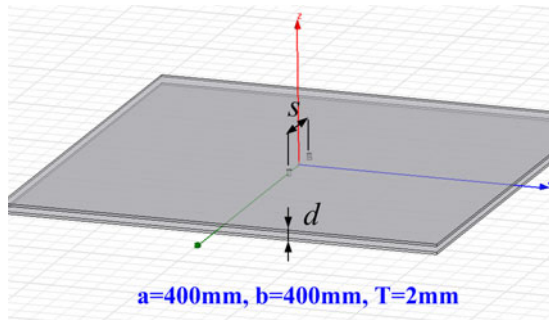


Fig. 3. Ansoft simulation model.

in the optimetrics analysis. Meanwhile, the skin effect needs to be taken into account. In the high-frequency spectrum, the conductor current is not uniformly distributed over the entire cross sectional area of the laminated busbar, but rather tends to be concentrated near the surface. The inductance varies with frequency as a result of the skin effect: it decreases at higher frequency because the flux linkage between conductor regions decreases. Taking into account the high frequency current skin distribution effect, according to the IGBT turn-off fall time, the **skin effect depth** is set as follows:

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_0}} = 0.0809 \text{ mm} \quad (5)$$

where the turn-off fall time of the test bench is $1.5 \mu\text{s}$, so f is equal to 667 kHz; ρ is the resistivity of copper, and μ_0 is the magnetic permeability. Fig. 3 depicts the Ansoft simulation model of a two-layer laminated busbar with CCL length s and insulation thickness d , and Fig. 4 shows the $L-s$ and $L-d$ optimetrics analysis curves.

Fig. 4(a) shows the $L-s$ simulation curve when the CCL length s varying from 25 mm to 150 mm, and Fig. 4(b) shows the $L-d$ simulation curve with the insulation thickness d varying from 1 to 4 mm. From coordinates of point m1 and m2, the slope of the curve can be measured as shown in Fig. 4. When s increase by one times from m1 ($s = 75 \text{ mm}$) to m2 ($s = 150 \text{ mm}$), the stray inductance increases from 5.2 to 7 nH. Meanwhile, when d increase by one times from m1 ($d = 2 \text{ mm}$) to m2 ($d = 4 \text{ mm}$), the stray inductance increases from 10 to 18 nH. Based on the Ansoft optimetrics analysis simulation results, the larger

the loop length s and insulation thickness d is, the larger the CCL stray inductance L is, and two conclusion points can be gained as:

- 1) when the CCL length s increases by one times, the CCL stray inductance L increases by 0.3 times, as shown in Fig. 4(a);
- 2) when the insulation thickness d increases by one times, the CCL stray inductance L increases by 0.8 times, as shown in Fig. 4(b).

Simulation results above results indicate that the stray inductance is significantly influenced by the CCL length and insulation thickness. Furthermore, the insulation thickness plays a more important role than the CCL length for the stray inductance. Therefore, a low stray inductance laminated busbar design should have close components layout and thin insulation layer.

B. Three-Layer Laminated Busbar

Because of different converter topologies, three-layer and multilayer laminated busbars are inevitably employed in high-power inverters. The three-layer laminated busbar is made up of three conducting plates with two dielectric layers, which is partly different from the two-layer laminated busbar. Regarding of the layout of the one more layer, there are two possible stacking structures of the three-layer laminated busbar, as depicted in Fig. 5:

- 1) the third layer is stacked inside of the two-layer laminated busbar [see Fig. 5(a)];
- 2) the third layer is stacked outside of the two-layer laminated busbar [see Fig. 5(b)].

From these two structures, two basic CCLs (where the basic CCL is formed by any two planar busbar layers) CCL1 and CCL2 of the three-layer laminated busbar can be obtained in Fig. 5. Furthermore, the $L-s$ and $L-d$ optimetrics analysis simulation models and curves of two CCLs are shown in Figs. 6 and 7, respectively. According to two coordinates of point m1 and m2 in the simulation curve, it is noticeable that the increasing rate of $L-s$ and $L-d$ curves are the same as that of the two-layer laminated busbar, which are 0.3 times and 0.8 times. Thus, the one more layer has no help to decrease the CCL stray inductance rising rate compared with the two-layer laminated busbar. However, if the two-layer laminated busbar has the same separation distance as the three-layer laminated busbar, it can be found that the stray inductance of CCL1 decreases by about 2.8% comparing inductances of point m1 and m2 in two $L-d$ curves [see Figs. 4(b) and 7(b)]. This is caused by the induced current of the third layer, as shown in Fig. 8(a) (the green color arrow with the scale of 10^4 A/m^2). This induced current decreases the stray inductance for the mutual effect. In Fig. 8(b), the induced unidirectional current is closed at infinity under this stacking structure. Obviously, the skin effect can be observed from the uniform induced current distribution around the lower surface of the third layer in the XZ plane view.

Furthermore, because the third layer increase the separation distance of CCL2 from $d = 2 \text{ mm}$ in two-layer to $(2 \cdot d + T) = 6 \text{ mm}$ in three-layer, the stray inductance of

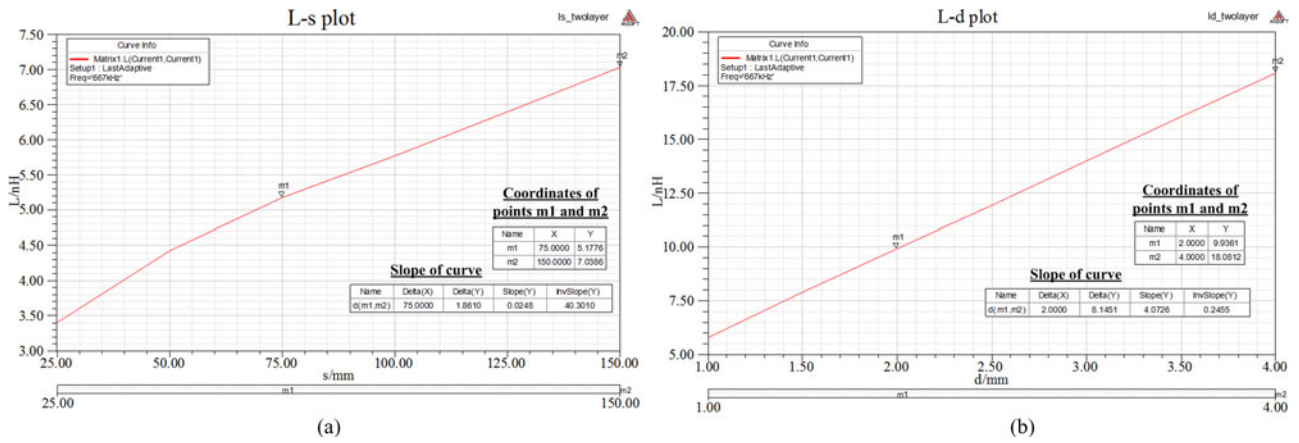


Fig. 4. Ansoft optimetrics analysis simulation curves. (a) L - s simulation curve. (b) L - d simulation curve.

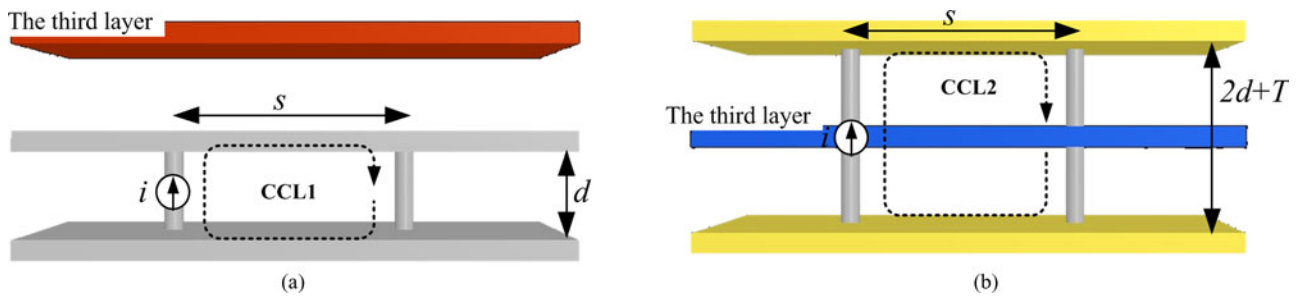


Fig. 5. Two basic CCLs of two structures in the three-layer laminated busbar: (a) CCL1. (b) CCL2.

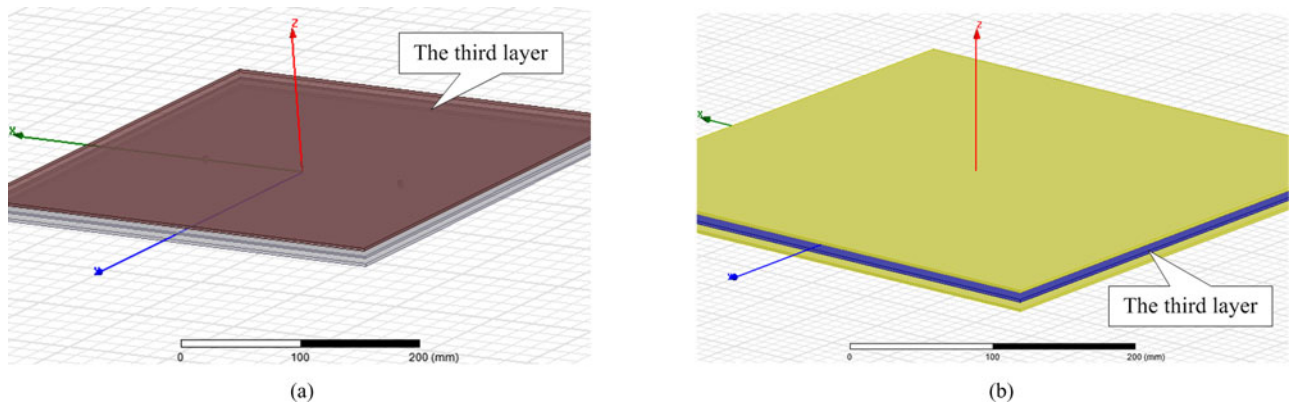


Fig. 6. Ansoft simulation models of two basic CCLs: (a) CCL1 and (b) CCL2.

CCL2 increases 111% [see Figs. 7(d) and 4(b)]. Whereas if the two-layer laminated busbar has the same separation distance ($2 \cdot d + T$) as CCL2, the stray inductance of CCL2 will have 12.8% lower than that of two-layer busbar with the ($2 \cdot d + T$). The reduction of the CCL stray inductance is due to the large induced current of the third layer as shown in Fig. 9 (the blue color arrow with the scale of 10^6 A/m²). This induced current is mainly caused by other two layers, via holes, and connecting screws. Moreover, the upper and lower surfaces of the third layer form a closed induced current loop under this laminated busbar stacking order as shown in Fig. 9(b).

Generally speaking, one CCL of a three-layer laminated busbar have these two basic CCLs in an inverter bridge, as shown in Fig. 10. S_1 and S_2 is the current commutation length of two CCLs, respectively. Fig. 10(a) consists of two basic CCL1, and Fig. 10(b) has two basic CCLs—CCL1 and CCL2—in one loop. In Fig. 10(a), the CCL can be totally treated as the basic CCL1 with length ($S_1 + S_2$) because of the small errors less than 6%. This small error is caused by the weak magnetic field coupling that can be neglected. The CCL [see Fig. 10(b)] is called as mixed CCL in here, which is formed by two basic CCLs—CCL1 and CCL2. The CCL length and the separation distance

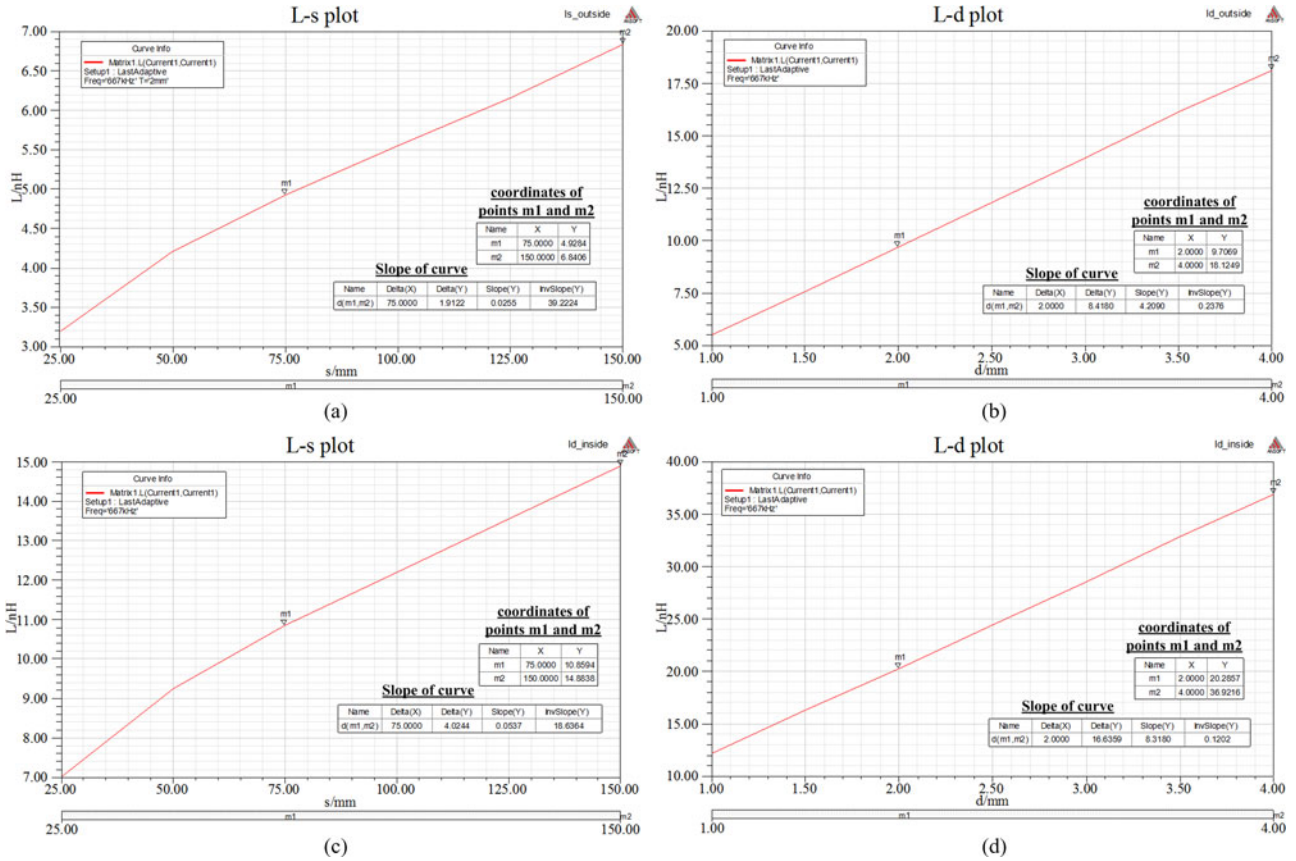


Fig. 7. Ansoft optimetrics analysis curves for two basic CCLs. (a) $L-s$ simulation curve of CCL1. (b) $L-d$ simulation curve of CCL1. (c) $L-s$ simulation curve of CCL2. (d) $L-d$ simulation curve of CCL2.

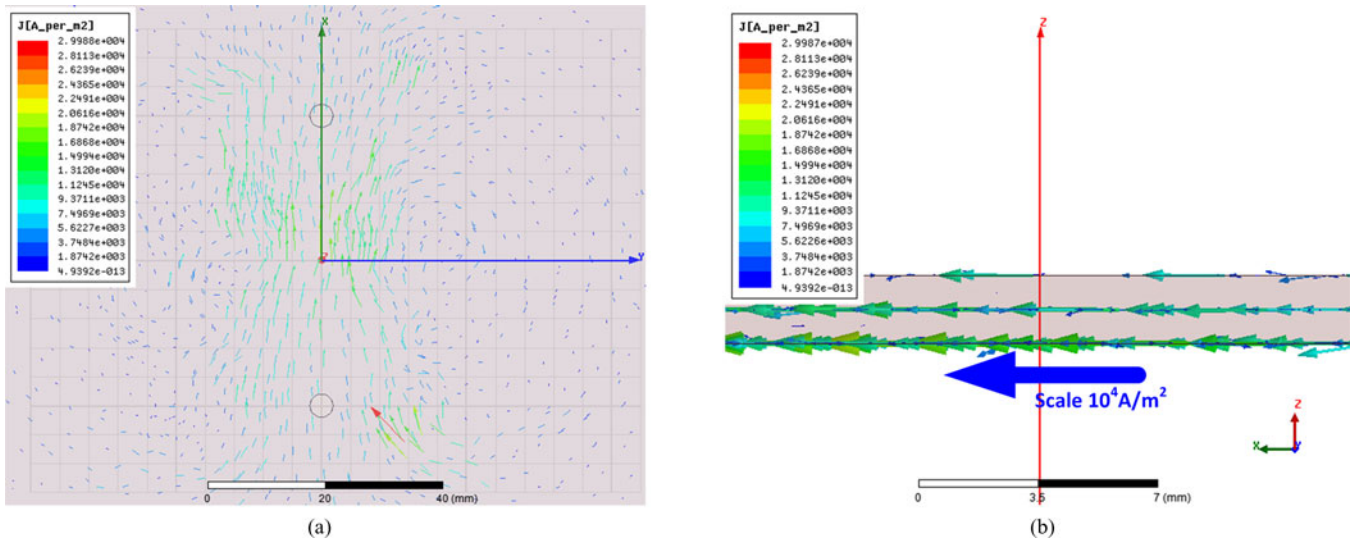


Fig. 8. Induced current distribution of CCL1. (a) XY plane view and (b) XZ plane view.

between layers in the mixed CCL of the three-layer laminated busbar are discussed in the following.

In order to investigate the mixed type CCL, a normalized three-layer laminated busbar CCL stray inductance $L_{three-layer}/$

$L_{two-layer}$ as function of S_1 and M is expressed as

$$\frac{L_{three-layer}}{L_{two-layer}} = f(S_1, M) \quad (6)$$

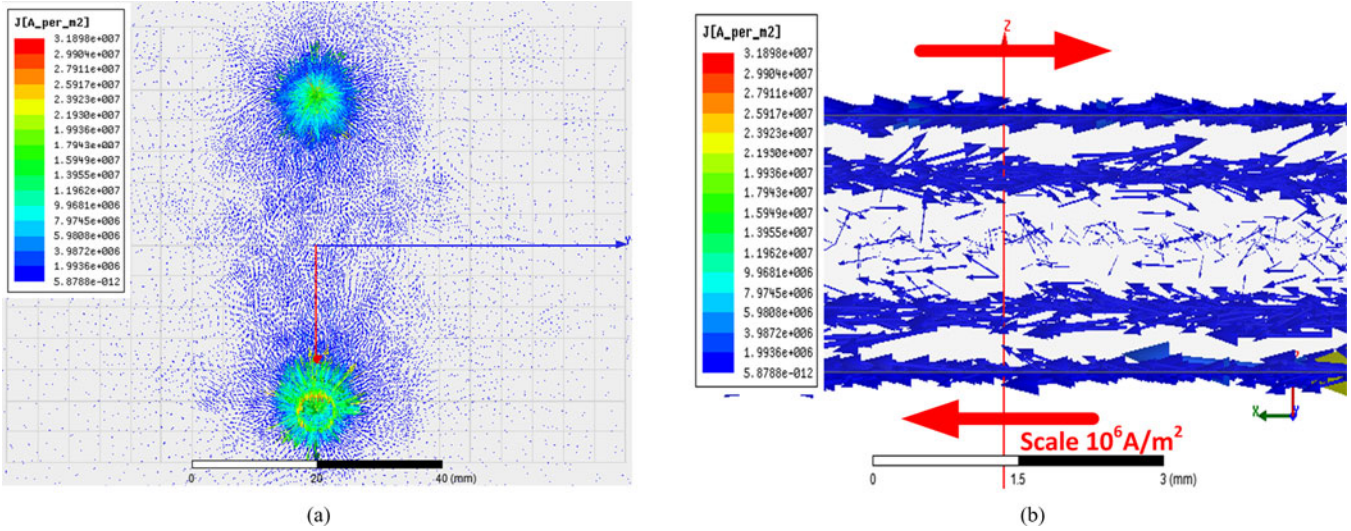
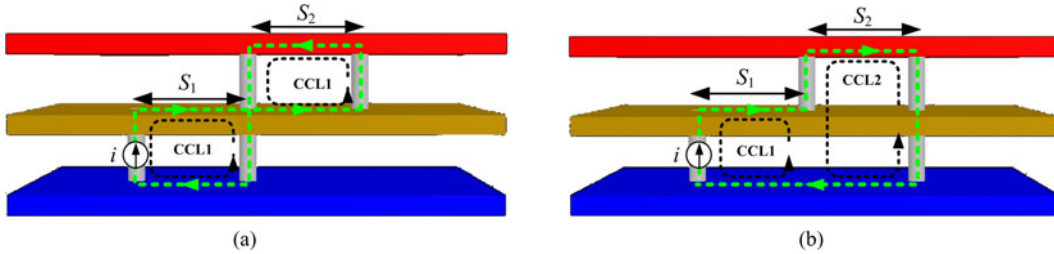
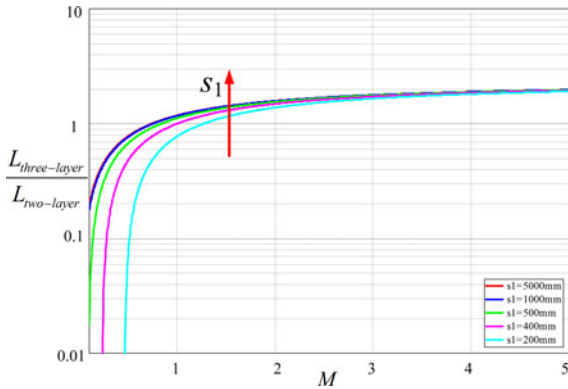

 Fig. 9. Induced current distribution of CCL2. (a) *XY* plane view and (b) *XZ* plane view.


Fig. 10. Two possible CCLs of three-layer laminated busbar. (a) Two basic CCL1 and (b) mixed CCL.


 Fig. 11. Three-layer busbar inductance curves in terms of M and S_1 .

where $L_{\text{three-layer}}$ is the stray inductance of mixed CCL of three-layer laminated busbar; $L_{\text{two-layer}}$ is the inductance of a two-layer laminated busbar with the same CCL length ($S_1 + S_2$) and separation distance d as CCL1; M is equal to S_2/S_1 . Fig. 11 shows the simulation result of the mixed CCL stray inductance in terms of M and S_1 . When $M \ll 1$, it indicates that S_2 is short enough to be neglected, $L_{\text{three-layer}}/L_{\text{two-layer}}$ is small. The CCL stray inductance $L_{\text{three-layer}}$ decreases rapidly for the dominant low stray inductance part of the basic CCL1. When $S_2/S_1 \geq 3$, $L_{\text{three-layer}}$ stabilizes at the maximum value for the predominant component of the basic CCL2, which conspicuously increases the stray inductance of the mixed CCL in the

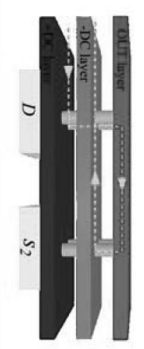
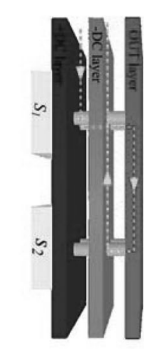
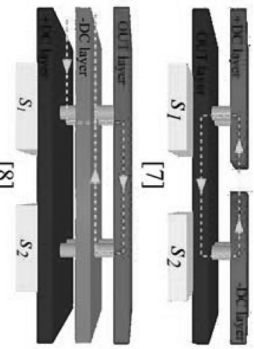
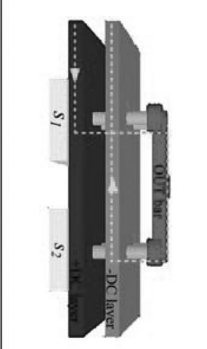
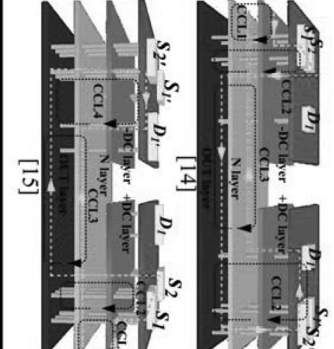
three-layer laminated busbar. Consequently, the basic CCL2 on one hand should not exceed 3 times of the basic CCL1, on the other hand maximize the proportion of the basic CCL1 to reduce the CCL stray inductance. Another conclusion can be summarized that simulation curves move upward due to the reduction of the nonlinear magnetic coupling.

Although the three-layer laminated busbar with the basic CCL1 has a positive effect on the stray inductance reduction, the one more layer raises the laminated busbar cost. Additionally, the three-layer laminated busbar with the basic CCL2 increases the busbar stray inductance. Hence, the best laminated busbar structure is the two-layer one that places IGBTs and dc capacitor bank departed into two sides presented in [7]. However, because of the limitations of IGBT packages (single-switch or dual-switch), dc-link capacitor types (metal film or electrolytic), and converter topologies (single-phase or three-phase), these side-by-side laminated busbar structures cannot be extensively applied to the high-power inverter applications.

C. Multilayer Laminated Busbar

The multilayer laminated busbar is required for that the current flows through multiple semiconductor devices in multilevel inverters. For example, the long CCL composes four semiconductor devices and six connecting nodes in the three-level NPC inverter [14], [15].

TABLE I
LAMINATED BUSBAR APPLICATIONS

References	Topologies	Structures	Layers	CCLs	Split plate layers	IGBT package	Device numbers
[1]	Buck converter		3	1	0	Chopper-switch	1
[3], [6]	Single-phase Half-bridge inverter		3	1	0	Single-switch	2
[7], [8]	Single-phase H-bridge inverter		2-3	2	1-2	Single-switch	4
[13]*	Three-phase H-bridge converter		2	3	0	Single-switch	6
[14]**, [15]**	Three-phase 3-level NPC converter		4	6	2	Dual-switch, Single-switch	12

* outputs is not planar busbar, but wires or copper strips which are directly connected with IGBT modules; ** literature has 2 CCLs in one bridge. So, there are totally 6 CCLs for three bridges.

The published papers have discussed several laminated busbar applications used in different topologies. Thus, considering the layers, CCLs, split plates (several plates are placed side-by-side in the same layer), semiconductor device numbers, and topologies, the laminated busbars can be summarized in Table I.

The yellow color block represents one IGBT or diode, and the green color dotted line shows the red dotted line CCL depicted in the circuit.

Among these various laminated busbar structures, it can be deduced that the number of layers is related with the connecting

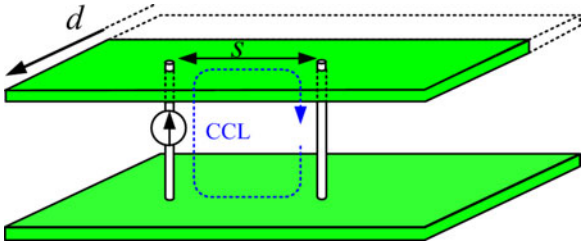
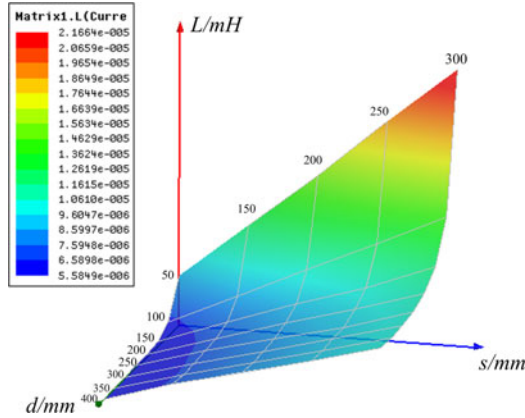


Fig. 12. Laminated busbar with split copper plate.

Fig. 13. Stray inductance L simulation results as the function of s and d .

nodes of different converters. The Buck converter, half-bridge, and single-phase/ three-phase H-bridge inverter have three connecting nodes (two dc-input nodes and one output node), as shown in [1], [3], [6], and [8]. Thus, the three-layer laminated busbar is utilized. Especially, as shown in [7], the dc inputs is placed side-by-side, so a two-layer laminated busbar is used for the reduced layer structure; as shown in [13], the output is connected by wires, so a two-layer laminated busbar with the output layer removed. Although [7] and [13] reduced layer and cost, these unique structures have narrow applications and may increase the CCL stray inductance. A balance between the cost and inductance is needed.

In multilevel inverters, several busbar planar plates are placed side-by-side in the same layer to reduce the multilayer laminated busbar layers in multilevel NPC inverters such as the outputs copper plates and dc inputs copper plates. This split plate can immensely reduce the laminated busbar cost. However, the split plate width should not be too short, and the FEA simulation of a two-layer laminated busbar with split plate demonstrates it, as shown in Fig. 12 ($a = 400$ mm, $b = 400$ mm, $T = 2$ mm). The stray inductance simulation results as the function of upper planar busbar width d and CCL (blue dotted line) length s are shown in Fig. 13. When d is larger than 200 mm, L raises slowly with the increase of s . Conversely, the L - s curve rises rapidly. Furthermore, the simulation results indicate that:

- 1) the longer CCL length s is, the larger stray inductance L will be;
- 2) the shorter width d is, the larger stray inductance L will be;

- 3) the plate width cannot be too short and d should be longer than 40%–50% of the busbar width, which means that one layer has two side-by-side split plates at most and best.

Although the structure of multilayer laminated busbar is related to many factors, following conclusions can be concluded for the multilayer laminated busbar design. For an n -level NPC inverter, there are the dc inputs and IGBT connecting nodes can use split layers connecting, which have $(n-1)$ layers; output phase and neutral clamping layers are whole and intact planar busbar, which have $(n-1)$ layers. So, there are totally $2(n-1)$ layers for an n -level NPC inverter, as three-level inverter shown in [14] and [15] (see Table I). Based on the result, taking a five-level NPC inverter as an example, the longest CCL in an eight-layer laminated busbar can be derived as shown Fig. 14. The phase output layer A and neutral clamping layer N_1 , N_2 , and N_3 are whole planar busbar layer, and IGBT connecting layers are 4 split plate layers.

For the CCL flowing through multiple semiconductor devices, the mixed CCLs are complex in the multilayer laminated busbar, which consists of more than three basic CCLs in one loop, as shown in Table I (one blue dotted circle represents one basic CCL). In order to get symmetrical CCL stray inductances, it is needed to augment the low inductance basic CCL and reduce the high inductance basic CCL by modifying busbar layers stacking order and semiconductor devices layout. Furthermore, the modification can get symmetrical stray inductances of CCLs.

IV. THREE-LAYER LAMINATED BUSBAR EXAMPLE

A. Three-Layer Laminated Busbar

A three-layer laminated busbar is designed to connect four IGBTs (Infineon FZ2400R17KF6 C B2) in a 75kVA single-phase H-bridge inverter. The photo and the structure of the laminated busbar are shown in Figs. 15 and 16, respectively. Fig. 16 depicts the physical structure of the three-layer laminated busbar. The laminated busbar is composed of three layers: the negative dc input bus (layer A), the positive dc input bus (layer B), and two ac outputs (layer C and D are located at the same layer).

Fig. 17 shows the current flowing paths of two CCLs in the laminated busbar, as analyzed in Section II. Assuming that the load current I_L is negative, the CCL1 [see Fig. 1(f)] inside of the laminated busbar is illustrated in Fig. 17(a) during T_2 turn-off transients. The negative load current I_L is divided into two currents. T_1 FWD current i_{T_1} flows from layer C to layer B, and T_2 current i_{T_2} flows from layer C to layer A. From the current paths, it shows that the CCL1 contains two CCL stray inductances l_{AB1} and l_{BC1} . When T_4 is turned off, the current flowing path of CCL2 [see Fig. 1(n)] is shown in Fig. 17(b). Likewise, the CCL2 contains two CCL stray inductances l_{AB2} and l_{AD2} . The positive load current I_L consists of T_3 FWD current i_{T_3} and T_4 current i_{T_4} . Furthermore, CCL1 is the type of basic CCL1 as analyzed in three-layer laminated busbar while CCL2 is the type of mixed CCL. Accordingly, the CCL1 has a lower stray inductance than CCL2 based on the conclusion in Section III.

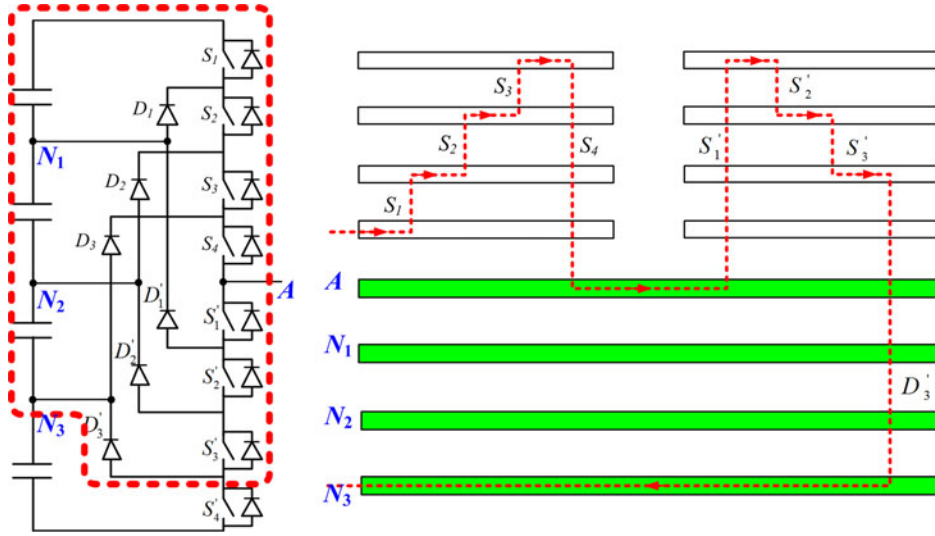


Fig. 14. Eight-layer laminated busbar for five-level NPC inverter with longest CCL.

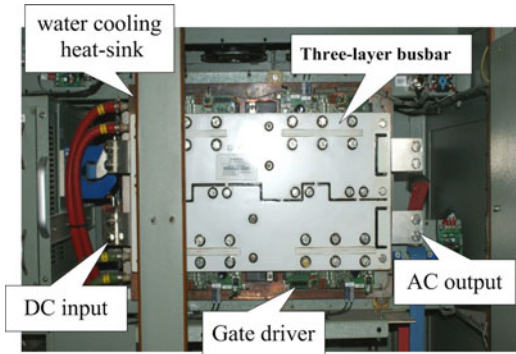


Fig. 15. Three-layer laminated busbar.

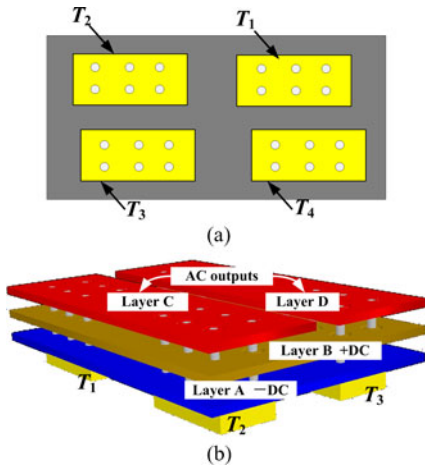


Fig. 16. Structure of the three-layer laminated busbar: (a) the top view and (b) the 3-D view.

B. Three-Layer Laminated Busbar FEA Modeling

Fig. 18 shows twoCCL simulation models (IGBTs are replaced by copper strips) of the three-layer laminated busbar. The dimensions of the layout are $536 \times 282 \times 12.8 \text{ mm}^3$. After necessary solver settings, the stray inductance is extracted

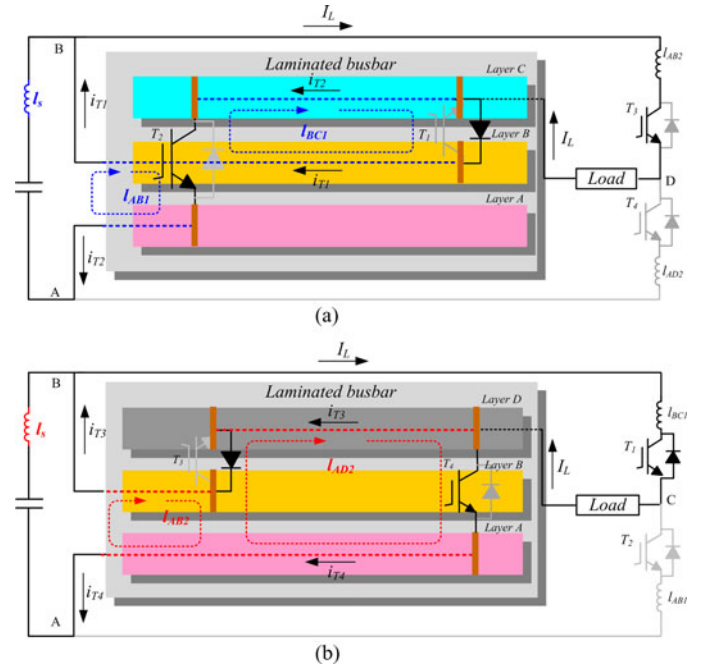


Fig. 17. Two CCL flowing paths of the original laminated busbar: (a) loop 1 and (b) loop 2.

from resistance and inductance (RL) matrix and the stray inductances of two loops can be obtained as: $L_{loop1} = 13.554 \text{ nH}$, $L_{loop2} = 20.7750 \text{ nH}$. The simulation results point out that the stray inductances of two CCLs are asymmetrical in the three-layer laminated busbar, which confirms the analysis in Section II.

V. EXPERIMENTAL RESULTS OF THREE-LAYER LAMINATED BUSBAR

A. Impedance Resonant Measurement-Method

To further verify the asymmetry of CCL stray inductances in the three-layer laminated busbar, an accurate step-by-step

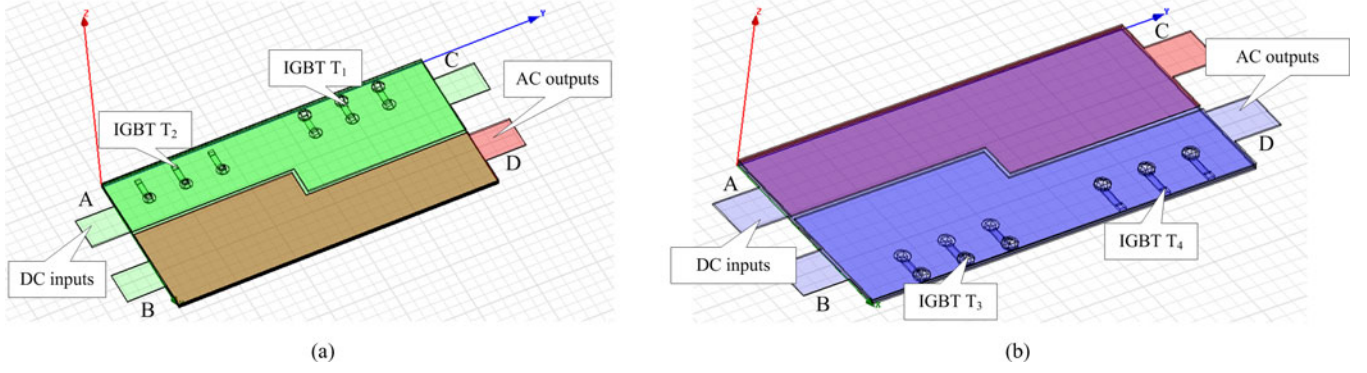


Fig. 18. Simulation models of two CCLs of the three-layer laminated busbar: (a) model of loop1 and (b) model of loop2.

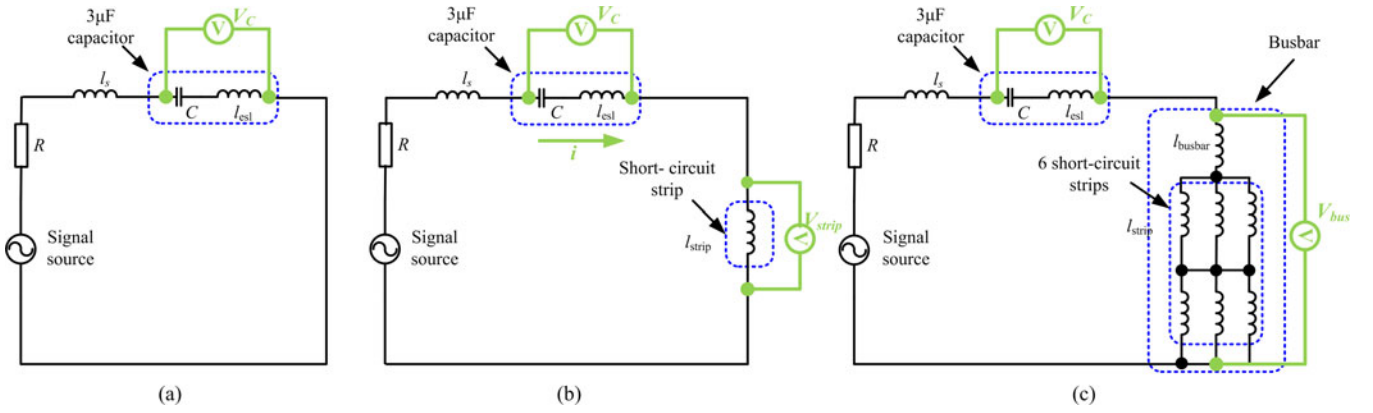


Fig. 19. Laminated busbar CCL stray inductance measurement processes: (a) step 1, (b) step 2, and (c) step 3.

measurement method based on the impedance resonance is proposed in this section. Fig. 19 shows the schematic for the stray inductance extraction method. A $3\ \mu\text{F}$ polypropylene film capacitor C and a $50\ \Omega$ current limiting resistor R are connected to the laminated busbar with IGBT short-circuit copper strips. The capacitor and stray inductances form an impedance resonant series circuit. l_{esl} is the ESL of capacitor C , l_{strip} is the stray inductance of short-circuit copper strip, l_{busbar} is the CCL stray inductance of laminated busbar, and l_s is the other circuit parasitic inductance (connecting wires and ESL of R). A variable frequency sinusoidal voltage signal is injected by Agilent33210 A signal generator. The detail stray inductance extraction processes are described as follows.

Step 1: The ESL of capacitor C is first measured by an independent test as shown in Fig. 19(a). When the measured voltage V_c reaches the minimum value by adjusting the frequency of the input signal, the following relationship can be obtained:

$$\frac{1}{2\pi f_a C} = 2\pi f_a l_{esl} \quad (7)$$

where f_a is the resonant frequency of step 1.

Step 2: The short-circuit copper strip is series with the capacitor C and resistor R as shown in Fig. 17(b). While the capacitor voltage V_c is equal to the short-circuit copper strip voltage V_{strip} by varying the frequency of the input signal, the relationship is

given as

$$\begin{aligned} V_C &= \left(\frac{1}{2\pi f_b C} - 2\pi f_b l_{esl} \right) \cdot i \\ V_{strip} &= 2\pi f_b l_{strip} \cdot i \\ V_C &= V_{strip} \end{aligned} \quad (8)$$

where f_b is the resonant frequency of step 2. Hence, the following impedance relationship can be given:

$$\frac{1}{2\pi f_b C} - 2\pi f_b l_{esl} = 2\pi f_b l_{strip}. \quad (9)$$

Equation (9) illustrated that the capacitor impedance is equal to the short-circuit copper strip inductive impedance.

Step 3: Fig. 17(c) shows the laminated busbar installed with short-circuit copper strips equivalent circuit. Adjust the input signal frequency, until the voltage V_c across the capacitor is equal to the laminated busbar voltage V_{bus} . As the one IGBT module has three short-circuit copper strips, the following impedance relationship can be expressed as:

$$\frac{1}{2\pi f_c C} - 2\pi f_c l_{esl} = \frac{4}{3}\pi f_c l_{strip} + 2\pi f_c l_{busbar} \quad (10)$$

where f_c is the resonant frequency of step 3.

From (7)–(10), the CCL stray inductance of the laminated busbar can be derived as

$$l_{busbar} = \frac{1}{4\pi^2 f_c^2 C} - \frac{1}{6\pi^2 f_b^2 C} - \frac{1}{12\pi^2 f_a^2 C}. \quad (11)$$

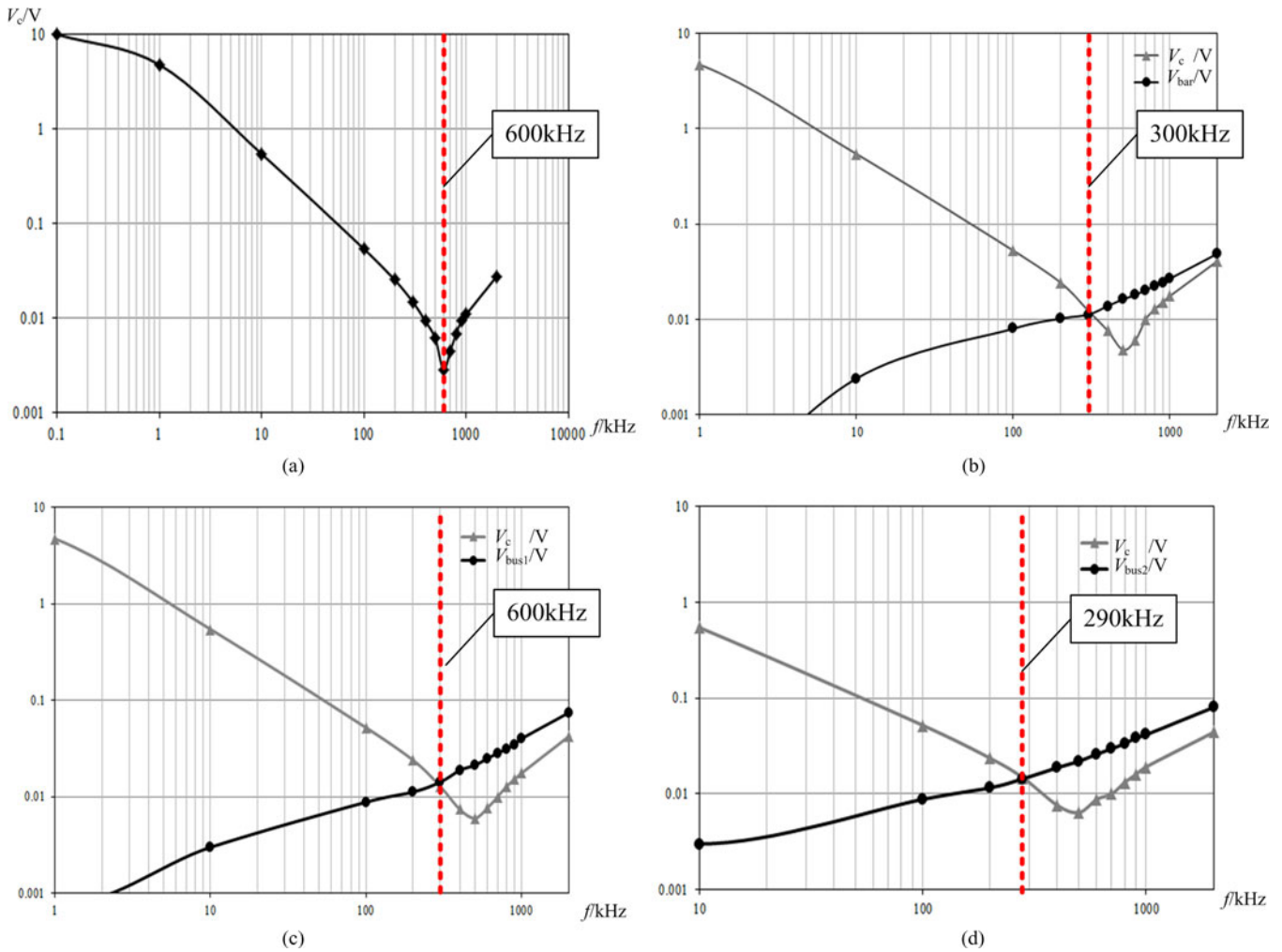


Fig. 20. Measured voltage–frequency curves: (a) step 1, (b) step 2, (c) step 3 for loop 1, and (d) step 3 for loop 2.

TABLE II
INDUCTANCE MEASUREMENT AND SIMULATION RESULTS

Method	L_{loop1} (nH)	L_{loop2} (nH)
Measurement	14.2	20.78
Simulation	13.6	20.8

The measured voltage–frequency curves of three steps are shown in Fig. 20. When the capacitor voltage V_c reaches the minimum value by varying the frequency of input signal source in step 1, the frequency f_a at this time is 600 kHz as shown in Fig. 20(a). In step 2, the capacitor voltage V_c (the gray line with triangle marker) and the short-circuit copper strip voltage V_{strip} (the black line with circle marker), as shown in Fig. 20(b), have the equivalent value at the frequency $f_b = 300$ kHz. Two CCLs stray inductance are measured in step 3 as shown in Fig. 20(c) and (d). The frequency f_c of the capacitor voltage V_c (the gray line with triangle marker) and the two busbar voltage $V_{bus1/2}$ of CCLs (the black line with circle marker) are 300 and 290 kHz, respectively.

Applying (11), the stray inductance of two CCLs can be obtained in Table II. It can be seen that the induced inductance l_s does not affect the measuring results, and two CCL stray

inductances measuring results are 14.2 and 20.78 nH, which have a good agreement with the Ansoft simulation results in Section IV. Thus, the measurement results demonstrate high accuracy of this improved method.

B. Overvoltage Across IGBTs

From the above stray inductance measurement results, the stray inductances of two CCLs are unequal. From the point of view of CCL stray inductances in the inverter circuit, these dissymmetrical stray inductances cause that IGBTs of the larger stray inductance CCL sustaining higher voltage and thermal stresses than that of the other CCL. Fig. 21 shows the experimental results of IGBT voltage overshoot waveforms in two CCLs. The IGBT voltage overshoot of CCL1 is higher than CCL2 about 10 V in unloaded condition and 40 V with 60 kW load, which verifies the stray inductance asymmetry of two CCLs in the three-layer laminated busbar.

VI. DISCUSSION

Based on the investigation of the laminated busbar, a compromised optimum laminated busbar structure scheme of the

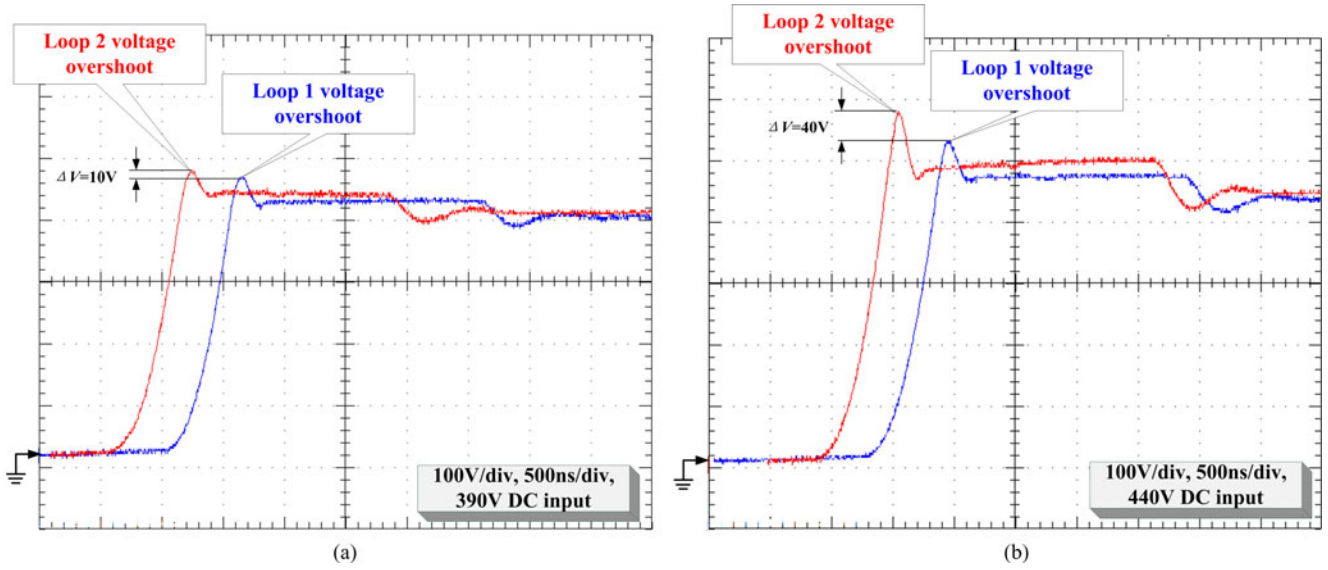


Fig. 21. IGBT voltage overshoots of two CCLs: (a) unloaded condition and (b) 60 kW load condition.

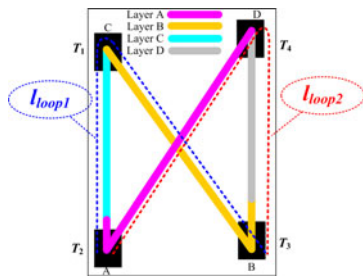


Fig. 22. Current commutation length of two CCLs.

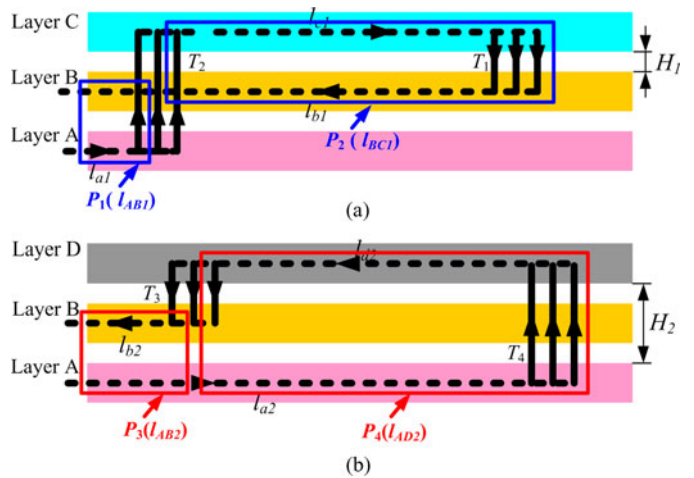


Fig. 23. Separation distance of CCLs: (a) CCL1 and (b) CCL2.

proposed three-layer laminated busbar is proposed by FEA simulations in this section.

In view of the three-layer laminated busbar analysis results in Section III, the reasons why the analyzed busbar has the asymmetrical CCL stray inductance can be shown in Figs. 22 and 23. It can be seen that the asymmetrical CCL stray inductance is resulted from the device asymmetric layout (see the length of green and blue line in Fig. 22), as well as the asymmetric current loop separation distance between two layers (see the blue regions in Fig. 23). The P_1 and P_2 regions of CCL1 have the same separation distance H_1 between two layers, but the P_4 region of loop2 has a 2 times separation distance H_2 between layer A and layer D. Since the weakness asymmetric of IGBT layout, the effect of CCL length can be neglected. Moreover, while CCL1 is the basic CCL1 with a low stray inductance ($l_{AB1} + l_{BC1}$), CCL2 is the mixed CCL with a large CCL stray inductance ($l_{AB2} + l_{AD2}$) for $S_2 > S_1$. As a result, the stray inductance of CCL2 is larger than CCL1.

In order to balance the stray inductances of two CCLs, a tradeoff optimal design scheme is proposed by changing the stacking order of layer B and layer CD as shown in Fig. 24. Thus, Two CCLs are both the mixed CCL2, which have the same length and separation distance. Although the separation distance of P_1 region in the optimized CCL1 is longer than the original one, the separation distance of P_4 region in the optimized CCL2 is tremendously reduced. Meanwhile, the rise of CCL1 stray inductance is very small. Therefore, the optimized busbar structure decreases the stray inductance of CCL2 and makes the stray inductance of two CCLs equivalent. As shown in Table III, the simulation results indicate well symmetry of two CCLs.

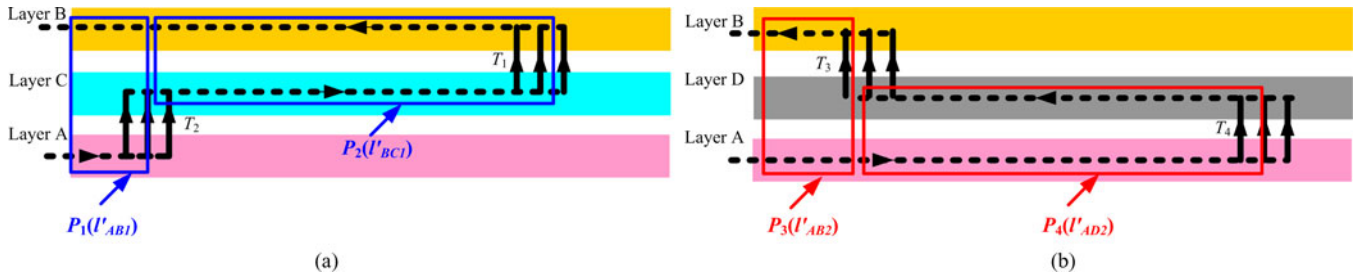


Fig. 24. Optimized laminated busbar CCLs: (a) loop 1 and (b) loop 2.

TABLE III
ORIGINAL AND OPTIMIZED LAMINATED BUSBAR SIMULATION RESULTS

Original three-layer busbar		Optimized three-layer busbar	
L_{loop1} (nH)	L_{loop2} (nH)	L_{loop1} (nH)	L_{loop2} (nH)
13.6	20.8	15.07	15.78

VII. CONCLUSION

In this paper, analytical CCL shows new feature that the laminated busbar stray inductance results in the CCL stray inductance asymmetry. Ansoft FEA simulation is utilized to investigate the two-layer, three-layer, and multilayer laminated busbars. Considering topologies and physical structures, the CCL stray inductances of different layer laminated busbar are proposed and analyzed. It is shown that the skin effect, mutual effect, CCL length, CCL separation distance, and split plate significantly influence the stray inductance of laminated busbar. Moreover, the multilayer laminated busbar is introduced for multilevel NPC inverters.

Based on the investigation results, the CCL stray inductances of a three-layer laminated busbar, which is used in a high power single-phase H-bridge inverter, are extracted by means of the FEA simulation and an accurate step-by-step impedance resonant measurement-method. Furthermore, IGBT voltage overshoot waveforms validate the stray inductances asymmetry of the laminated busbar. A compromise scheme between the stray inductance and symmetry for the three-layer laminated busbar is proposed. In summary, a low and symmetrical stray inductance laminated busbar has following design guidelines:

- 1) laminated busbar CCL insulation distance should be designed as short as possible under the premise of insulation requirements;
- 2) laminated busbar layers should be placed as close as possible under the premise of thermal and temperature requirements;
- 3) laminated busbar CCLs should be designed symmetrically by modifying semiconductor device layout and stacking order.

REFERENCES

- [1] J. L. Schanen, E. Clavel, and J. Roudet, "Modeling of low inductive busbar connections," *IEEE Ind. Applicat. Mag.*, vol. 2, no. 4, pp. 39–43, Sep./Oct. 1996.
- [2] H. J. Beukes, J. H. R. Enslin, and R. Spee, "Busbar design considerations for high Power IGBT converters," in *Proc. 12th APEC*, 1997, pp. 847–853.
- [3] Z. Lounis and B. Davat, "Minimization of wiring inductance in high power IGBT inverter," *IEEE Trans. Power Del.*, vol. 15, no. 2, pp. 551–555, Apr. 2000.
- [4] M. A. Vogelsberger, T. Wiesinger, and H. Ertl, "Life-cycle monitoring and voltage-managing unit for DC-link electrolytic capacitors in PWM converters," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 493–503, Feb. 2011.
- [5] K. Fink and S. Bernet, "Advanced gate drive unit with closed-loop di_C/dt control," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 2587–2595, May 2013.
- [6] M. C. Caponet, F. Profumo, R. W. D. Doncker, and A. Tenconi, "Low stray inductance bus bar design and construction for good EMC performance in power electronic circuits," *IEEE Trans. Power Electron.*, vol. 17, no. 2, pp. 225–231, Mar. 2002.
- [7] F. Zare and G. F. Ledwich, "Reduced layer planar busbar for voltage source inverters," *IEEE Trans. Power Electron.*, vol. 17, no. 4, pp. 508–516, Jul. 2002.
- [8] C. Chen, X.-J. Pei, S. Yunhao, L. Xinchun, L. Xinming, and K. Yong, "Modeling and optimization of high power inverter three-layer laminated busbar," in *Proc. 4th ECCE*, 2012, pp. 1380–1385.
- [9] P. Ranstad and H.-P. Nee, "On dynamic effects influencing IGBT losses in soft-switching converters," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 260–271, Jan. 2011.
- [10] R. Hausmann and I. Barbi, "Three-phase DC-AC converter using four-state switching cell," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1857–1867, Jul. 2011.
- [11] B. Gultekin and M. Ermis, "Cascaded multilevel converter-based transmission STATCOM: System design methodology and development of a 12 kV ± 12 MVar power stage," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4930–4950, Nov. 2013.
- [12] A. T. Bryant, K. K. Vadlapati, J. P. Starkey, A. P. Goldney, S. Y. Kandilidis, and D. A. Hinchley, "Current distribution in high power laminated busbars," in *Proc. 14th Eur. Conf. EPE*, 2011, pp. 1–10.
- [13] H. Wen and W. Xiao, "Design and optimization of laminated busbar to reduce transient voltage spike," in *Proc. 21th ISIE*, 2012, pp. 1478–1483.
- [14] J. Wang, B. Yang, J. Zhao, Y. Deng, X. He, and X. Zhixin, "Development of a compact 750 KVA three-phase NPC three-level universal inverter module with specifically designed busbar," in *Proc. 25th APEC*, 2010, pp. 1266–1271.
- [15] L. Popova, T. Musikka, R. Juntunen, M. Lohtander, P. Silventoinen, O. Pyrhonen, and J. Pyrhonen, "Modeling of low inductive busbars for medium voltage three-level NPC inverter," in *Proc. IEEE PEMWA 2012*, pp. 1–7.
- [16] F. Z. Peng, W. Jin, Z. Fan, and Q. Zhaoming, "Development of a 1.5 MVA universal converter module for traction drive and utility applications," in *Proc. PESC*, 2005, pp. 2290–2295.
- [17] H. Zhu, A. R. Hefner, and J.-S. Lai, "Characterization of power electronics system interconnect parasitics using time domain reflectometry," *IEEE Trans. Power Electron.*, vol. 14, no. 4, pp. 622–628, Jul. 1999.
- [18] J. M. Guichon, J. Aime, J. L. Schanen, C. Martin, J. Roudet, E. Clavell, M. Arpilliere, R. Pasterczyk, and Y. Le Floch, "Busbar design: How to spare nanohenries?," in *Proc. Conf. IEEE IAS Annu. Meeting*, 2006, pp. 1865–1869.
- [19] C. M. R. J. Pasterczyk, J.-M. Guichon, and J.-L. Schanen, "Planar busbar optimization regarding current sharing and stray inductance minimization," in *Proc. Eur. Conf. on EPE-ECCE*, 2005, pp. 1–9.
- [20] Ansys Ansoft Maxwell2D/3D software, Ansoft (2010). [Online]. Available: <http://www.ansoft.com/>
- [21] F. Zare and G. Ledwich, "A plane busbar impedance calculation using MAXWELL's equations," in *Proc. 11th ISH*, 1999, pp. 2.148.P6–2.151.P6.



Cai Chen was born in Hubei Province, China. He received the B.E. degree in electrical and electronic engineering from Huazhong University of Science and Technology, Wuhan, China, in 2008.

He is currently with Huazhong University of Science and Technology. His current research interests include high-power inverters, high-power density, high-frequency power conversion, and electromagnetic interference.



Yu Chen (S'09–M'11) received the B.E. and Ph.D. degrees in electrical and electronic engineering from Huazhong University of Science and Technology, Wuhan, China, in 2006 and 2011, respectively.

From March 2008 to March 2009, he was an Intern in GE Global Research Center, Shanghai, China. In September 2011, he joined Huazhong University of Science and Technology as a Lecturer. His current research interests include the power electronic converter topologies, soft switching techniques, converter modeling, the fault diagnosis techniques, and the wind energy power-conversion system.



Xuejun Pei (M'12) received the B.E., M.E., and Ph.D. degrees in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 1998, 2001, and 2004, respectively.

In 2004, he joined Huazhong University of Science and Technology as a Teaching Assistant, where he has been an Associate Professor with the College of Electrical and Electronic Engineering since 2006. From March 2011 to March 2012, he was a Visiting Scholar at Michigan State University, East Lansing, USA. His research interests focus on high-power con-

verter, EMC issue, fault diagnosis of power electronics, and the related control techniques.



Yong Kang was born in Hubei Province, China, on October 16, 1965. He received the B.E. M.E, and Ph.D. degrees from Huazhong University of Science and Technology, Wuhan, China, in 1988, 1991 and 1994, respectively.

In 1994, he joined Huazhong University of Science and Technology as a Lecturer and was promoted to Associate Professor in 1996 and to Full Professor in 1998. He is currently the Head of the College of Electrical and Electronic Engineering, Huazhong University of Science and Technology. He is the au-

thor or coauthor of more than 60 technical papers. His current research interests include power electronic converter, ac drivers, electromagnetic compatibility, and their digital control techniques.